REMARKS

Claims 1-20 were examined and reported in the Office Action. Claims 1, 2, 19 and 20 are rejected. New claims 21-25 are added. Claims 1 and 19 are amended. Claims 1-25 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 102

A. It is asserted in the Office Action that claims 1 is rejected under 35 U.S.C. § 102(e), as being anticipated by U. S. Patent Application No. 2004/0078701 issued to Miyanishi ("Miyanishi"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131,

> '[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Miyanishi discloses a semiconductor memory unit including a repair circuit. It is asserted in the Office Action that the ready signal generating circuit 51 of Fig. 1 in Miyanishi corresponds to the comparator delay modeling block of Applicant's claimed invention. It is also asserted in the Office Action that a repair selection signal generator 6 of Fig. 1 in Miyanishi corresponds to the repair circuit controller of Applicant's claimed invention. The repair circuit controller in Applicant's claimed invention directly receives the delayed enable signal from the comparator delay modeling block, whereas in Miyanishi the repair selection signal generator 6 can not directly receive an output 51 of the ready signal generating circuit 51.

Applicant asserts that Miyanishi does not teach, disclose or suggest Applicant's amended claim 1 limitations of

> a comparator modeling block for modeling a replica time for a predetermined time corresponding to address comparing times of the address comparators to delay the enable signal for the replica time; and a repair circuit controller in response to the delayed enable signal output from the comparator modeling block for generating one of a repair address enable signal and a normal address enable signal based on a comparison result of the address comparators.

Therefore, since Miyanishi does not teach, disclose or suggest all of Applicant's amended claim 1 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to Miyanishi. Thus, Applicant's amended claim 1 is not anticipated by Miyanishi.

Additionally, Applicant notes that Miyanishi also does not teach, disclose or suggest Applicant's new claim 21 limitations of

> a modeling block for modeling a replica time for a predetermined time corresponding to address comparing time of the address comparator to delay the enable signal for the replica time; and a repair circuit controller for generating one of a redundancy circuit and a normal circuit according to the result of the comparison in response to the delayed enable signal output from the comparator modeling block,

nor Applicant's amended claim 24 limitations of "comparing the input address with the stored repair address in response to the enable signal; modeling a replica time for a predetermined time corresponding to address comparing time of the address comparator; delaying the enable signal for the replica time." Therefore, Applicant asserts that since Miyanishi does not teach, disclose or suggest all of Applicant's new claims 21 and 24 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) could not be adequately set forth relative to Miyanishi. Thus, Applicant's new claims 21 and 24 can not be anticipated by Miyanishi. Additionally, the claims that directly or indirectly depend on new claims 21 and 24, namely claims 23-23, and 25, respectively, could also not be found to be anticipated by Miyanishi for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(e) rejection for claim 1 is respectfully requested.

B. It is asserted in the Office Action that claims 1, 2, 19-20 are rejected under 35 U.S.C. § 102(b), as being anticipated by U. S. Patent No. 6,223,248 issued to Bosshart ("Bosshart"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

Bosshart discloses memory devices and methods for re-mapping memory row redundancy during cache access. It is asserted in the Office Action that Bosshart discloses a comparator delay modeling block. Bosshart, however, does not show any circuit corresponding to Applicant's claimed comparator modeling block. That is, in Bosshart, there is no circuit modeling time needed to compare a repair address with an input address.

That is, Bosshart does not teach, disclose or suggest Applicant's amended claims 1 and 19 limitations of

> a comparator modeling block for modeling a replica time for a predetermined time corresponding to address comparing times of the address comparators to delay the enable signal for the replica time; and a repair circuit controller in response to the delayed enable signal output from the comparator modeling block for generating one of a repair address enable signal and a normal address enable signal based on a comparison result of the address comparators,

Therefore, since Bosshart does not teach, disclose or suggest all of Applicant's amended claims 1 and 19 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(b) has not been adequately set forth relative to Bosshart. Thus, Applicant's amended claims 1 and 19 are not anticipated by Bosshart. Additionally, the claims that directly or indirectly depend on claims 1 and 19, namely claims 2, and 20, respectively, are also not anticipated by Bosshart for the same reason.

Additionally, Applicant notes that Bosshart also does not teach, disclose or suggest Applicant's new claim 21 limitations of

> a modeling block for modeling a replica time for a predetermined time corresponding to address comparing time of the address comparator to delay the enable signal for the replica time; and a

> repair circuit controller for generating one of a redundancy circuit and a normal circuit according to the result of the comparison in response to the delayed enable signal output from the comparator modeling block,

nor Applicant's amended claim 24 limitations of "comparing the input address with the stored repair address in response to the enable signal; modeling a replica time for a predetermined time corresponding to address comparing time of the address comparator; delaying the enable signal for the replica time." Therefore, Applicant asserts that since Bosshart does not teach, disclose or suggest all of Applicant's new claims 21 and 24 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(b) could not be adequately set forth relative to Bosshart. Thus, Applicant's new claims 21 and 24 can not anticipated by Bosshart. Additionally, the claims that directly or indirectly depend on new claims 21 and 24, namely claims 23-23, and 25, respectively, could also not be found to be anticipated by Bosshart for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(b) rejections for claims 1, 2, and 19-20 are respectfully requested.

II. Allowable Subject Matter

Applicant notes with appreciation the Examiner's assertion that claims 3-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully asserts that claims 1-25, as they now stand, are allowable for the reasons given above.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-25 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: September 6, 2007

By: _____

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

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Jean Svoboda Date: September 6, 2007